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A Frequency Synthesizer with Low Phase Noise in UHF RFID Reader Based on Sigma-Delta Modulation Fractional Frequency Phase-Locked Loop

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Abstract. According to the frequency emission characteristics and related specifications of Ultra High Frequency (UHF) radio frequency identification (RFID), the RFID frequency synthesizer puts forward higher requirements on the noise and spurious suppression of the phase-locked loop. Its performance directly affects the sensitivity and stability of the receiver. How to design a high-performance and low-noise direct digital frequency synthesizer is a hot research topic in the industry. Firstly, the system design scheme of frequency synthesizer in UHF RFID reader based on sigma-delta modulation fractional frequency phase-locked loop is proposed. Secondly, the design advantages of digitization, large loop bandwidth, high precision and stability, are discussed. Thirdly, the generation source of phase noise is studied in detail, and the noise contribution of each component of the frequency synthesizer including signal source, loop filter, phase detector and charge pump, voltage controlled oscillator, ∑Δ modulator, etc. is simulated one by one. Finally, according to the most stringent ETSI EN 302 208-l emission spectrum specification of multiple radio frequency identification protocols, the frequency synthesizer phase noise requirement is less than -104dBc/Hz@200k Hz and -125dBc/Hz@1M Hz. And in this solution, experimental results show that the phase noise is only -116dBc/Hz@ 200k Hz and -132dBc/Hz@ 1M Hz, which not only meets the requirements of the specification, but also has a large margin space.

Keywords: delta sigma modulator, frequency synthesizer, phase noise, radio frequency identification (RFID) reader, ultra-high frequency band (UHF)

1 Introduction

RFID is a non-contact automatic identification technology that automatically identifies target objects and acquires relevant data through Radio Frequency (RF) signals. UHF RFID uses electromagnetic backscatter coupling, with main frequencies of 433 MHz, 860-960 MHz, 2.45 GHz and 5.8 GHz and so on. The UHF band from 860 MHz to 960 MHz is discussed in this paper. The radio frequency identification system is basically composed of radio frequency tags and readers. In the RFID system, the main influence on the cost and performance of the system is the reader.

EPC global™ Class-1 Generation-2 [1] and ISO 18000-6C [2] are the important UHF (860 MHz to 960 MHz) RFID standards, which define the air interfaces, and widely adapted by the industry. The limitations on spurious emissions specifications for UHF RFID systems mainly include European ETSI EN 302 208-l [3], North American FCC Title 47, Part 15 standards [4] and China's Radio Frequency Identification (RFID) Technology Application Regulations for 800/900MHz Band (Trial) [5]. It has been found that the ETSI standard has the most stringent requirements on the spectrum of the transmitter. According to the ETSI EN 302 208-l emission spectrum specification of multiple RFID protocols, the phase noise requirement of the frequency synthesizer can be calculated to be less than about -104dBc/Hz@200k Hz and -125dBc/Hz@1M Hz [6-10].

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In the system design of the RFID reader, the direct down-conversion structure is gradually accepted because of its superior on-chip integration. Furthermore, new requirements have been put forward for the frequency synthesizer. For a frequency synthesizer with low phase noise, proper system modeling is essential. It is necessary to carry out meticulous optimization design of each module circuit such as analog, RF, digital, etc., and fully consider a series of problems such as substrate isolation, high-frequency signal routing, high performance and low power consumption in CMOS system integration. Lu et al. [11-13] designed a constant-tuned gain voltage controlled oscillator (VCO) and a programmable charge pump (CP) based on the stable loop bandwidth. A stable loop bandwidth has some benefit to phase noise [14-15], but such a design introduces more capacitance. To PLL frequency synthesizer technology, the integer frequency division synthesizer has the disadvantages of very small loop bandwidth, slow response speed and slow speed capture. Fractional frequency synthesizer can overcome this problem, but brings the problem of spur delusion [16-21]. In order to solve the problem, Tian et al. [18] proposed a low-phase-noise UHF band fractional-n frequency synthesizer, and Mai et al. [22-25] improved the problem of quantization noise folding to low frequencies due to nonlinearities, and Lai et al. proposed a digital to analog converter (DAC) based on Mash structure, which achieved significant noise reduction effects in the audio and video field, but did not apply its results to the RFID field [26-28]. However, these techniques only improve the impact of quantization noise on system noise performance. In order to achieve better phase performance, it is necessary to consider the contribution of all modules to system noise as a whole.

In this work, the system design scheme of frequency synthesizer in UHF RFID reader based on sigma-delta modulation fractional frequency phase-locked loop is proposed. In this paper, the noise source of each part of the phase-locked loop is modeled, and the influence of system noise is analyzed as a whole. The system design controls the spur delusion problem by using sigma-delta modulation technology while maintaining the advantages of high loop bandwidth, low locking time and high frequency resolution. Experiment shows that the whole phase noise of this design scheme is only -116dBc/Hz@ 200k Hz and -132dBc/Hz@ 1M Hz, which not only meets the requirements of the RFID specification, but also has a large margin space.

This paper is organized as follows. Section 2 describes the system design and methods, and analyzes the advantages and accuracy and stability of the phase-locked loop system, then discusses the design of the Multi Stage Noise Shaping (MASH) structure $\sum\Delta$ modulator. Section 3 discusses the various phase noises of the frequency synthesizer in detail, and analyzes and simulates various noise sources such as signal source noise, loop filter noise, VCO Noise, and modulator noise, and so on. Section 4 concludes the paper.

2 System Design and Methods

The PLL frequency synthesizer was created due to the fatal flaws of the direct analog frequency synthesizer and the application limitations of the direct digital synthesizer. In the integer frequency synthesizer, since the frequency accuracy and the reference frequency are the same, it is difficult to optimize the frequency accuracy and the lock time at the same time, because small frequency accuracy requires a small reference frequency. According to experience, in order to prevent the reference frequency leakage caused by the phase detector (PDF) sampling effect, the loop filter (LF) bandwidth should be at least 1/20 to 1/10 times the reference frequency. In narrowband applications, it will result in a smaller reference frequency and a larger division ratio. For example, for UHF RFID systems (860 to 960 MHz), the channel bandwidth is 200 kHz. If integer division is used, the reference frequency is 200 kHz and the division ratio is 4300 to 4800. A narrow loop bandwidth will result in increase in lock time. The large division ratio (N) increases 20lgN dB (about 73 dB) to the in-band noise of the input reference signal, phase detector, charge pump, and divider. The fractional frequency synthesizer can overcome the above shortcomings. By adopting fractional frequency division, its frequency resolution can be much smaller than the reference clock frequency, which leads to larger loop bandwidth, faster lock time and better noise characteristics. For the UHF RFID system, if the fractional-frequency design is adopted, when the 10MHz reference frequency is used, the division ratio is required to be only 86-96, and the in-band noise is improved by about 33dB compared with the integer division system. Moreover, the loop bandwidth only needs to be controlled within 1MHz, which will not affect the loop stability of the PLL and greatly improve the lock time.

But on the other hand, the normal fractional frequency design brings the problem of spur delusion [16-21]. In this paper, in order to solve this problem, the system design scheme uses a fractional-frequency PLL phase-locked loop technology based on ∑Δ modulation. As shown in Fig. 1.

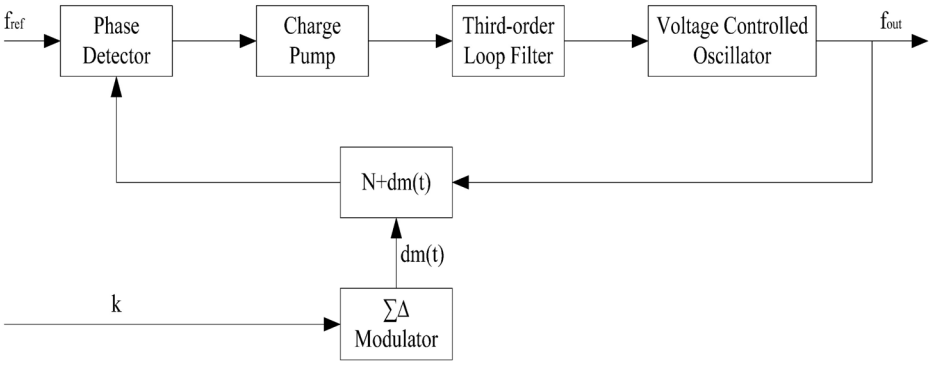

Fig. 1. Synthesizer System design based on ∑Δ modulation fractional frequency PLL technology

The system consists of phase detector, charge pump, third-order loop filter, voltage controlled oscillator, N+dm(t) frequency divider, and ∑Δ modulator. The ΣΔ modulator controls the frequency division ratio of the frequency divider. The instantaneous frequency division ratio is the sum of the basic frequency division ratio *N* and the output *dm(t)* from the ΣΔ modulator. The mean value of *dm(t)* is $k/2^m$, *m* is the bit width of the ΣΔ modulator. In the locked state, the output frequency and frequency accuracy satisfy the equations (1) and (2).

$$f_{out} = (N + \frac{k}{2^m}) \cdot f_{ref} . \tag{1}$$

$$\Delta f = \frac{1}{2^m} \cdot f_{ref} . \tag{2}$$

It can be seen that the bit width of the ΣΔ modulator can control the accuracy of the frequency. And the various output frequencies required can be obtained by different frequency division numbers N and integers input k. For example, if *fref* takes 10MHz, *N* takes 90, then an output frequency signal of 900MHz UHF band can be easily obtained. The loop bandwidth is as high as 200 kHz, and the fractional spur problem can be solved, and the requirements of the specification of UHF RFID are satisfied.

2.1 The Analysis of the Stability of Phase-locked Loop

The open-loop transfer function in this scheme is as shown in equation (3):

$$Ho(S) = \frac{Kpd \cdot Kvco \cdot F(s)}{N \cdot S} . \tag{3}$$

In equation (1), *Kpd* is the gain of the phase detector and the charge pump, *Kvco* is the conversion gain of the VCO, *N* is the division number, and *F(S)* is the transfer function of the loop filter. The loop filter adopts a third-order passive structure, as shown in Fig. 2, and its transfer function *F(S)* is as shown in equation (4).

$$F(S) = \frac{1 + sR_1C_1}{s(C_1 + C_2 + C_3)} \cdot \frac{1}{(1 + SR_1(C_2 + C_3))(1 + sR_2(C_2 // C_3))} . \tag{4}$$
$$C_1 >> C_2, C_3 \quad R_1 > R_2$$

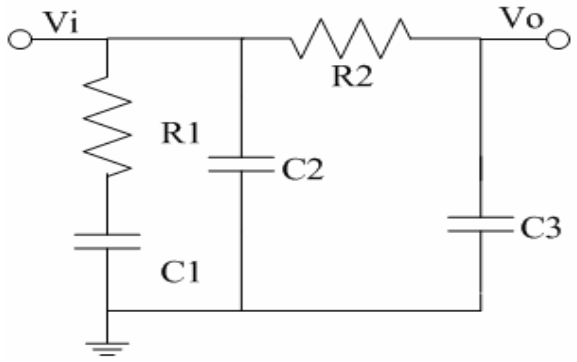

Fig. 2. Circuit diagram of third-order passive filter

The entire loop has become a 4-order phase-locked loop. The loop filter transmission characteristics will significantly affect the loop stability and noise transfer function. In addition to factors such as power consumption and integration, the design must also be combined with the specific parameters of other modules of the loop (such as charge pump) and circuit specific requirements (such as out-of-band filtering). In this design, typically *R1* takes 24k, *R2* takes 19k, *C1* takes 400pf, *C2* and *C3* take 22pf, and reference crystal frequency (*fref*) takes 10MHz, *N* takes 90, *Kpd* takes 30uA/(2л), and *Kvco* takes 40MHz/V. The simulated open-loop transfer characteristics according to equations (1) and (2) are shown in Fig. 3.

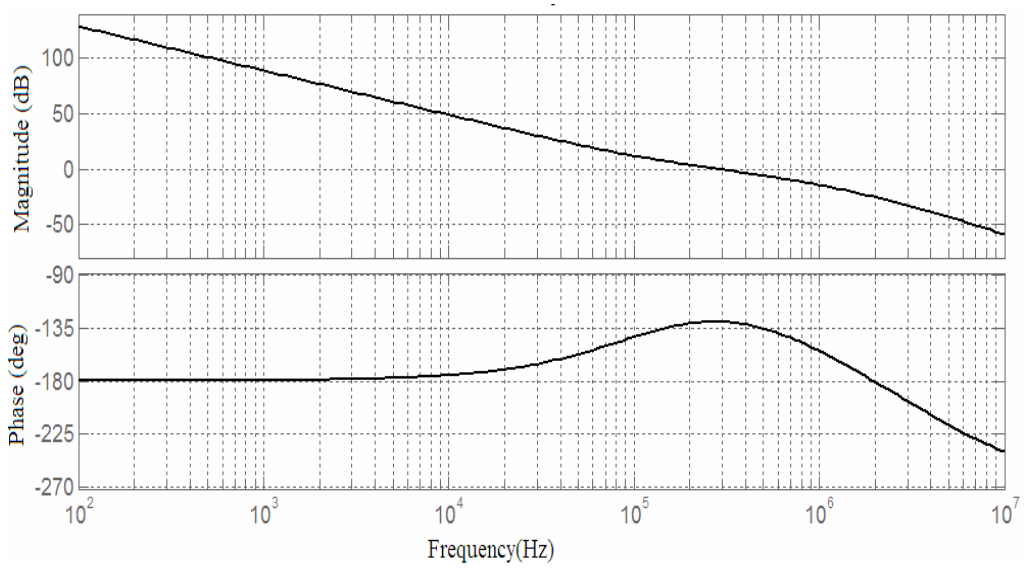

Fig. 3. Magnitude and phase spectrum of open-loop gain. As can be seen from this figure, when the open loop gain value is 1, the frequency value is 200 kHz, and the phase is -132 degree. This means that the loop bandwidth is 200 kHz and the phase margin is -132+180=48 degrees. So the phase-locked loop can work stably.

2.2 ∑Δ Modulator

In modern communication systems, the implementation of narrowband communication with compressed bandwidth is an inevitable trend, and its purpose is to make full use of limited spectrum resources. At the same time, the system requires that the switching among communication channels must be fast enough, which requires that the loop bandwidth must be large enough. The fractional-frequency phase-locked loop frequency synthesizer can achieve these requirements, but its disadvantage is that the periodic frequency division method will generate fractional spurs at the edge of the channel. The solution in this paper is to use ∑Δ modulation to randomize the division factor while pushing the quantization noise to the high frequency band, then the high frequency noise will be suppressed by the loop filter with low-

pass characteristics, therefore, fractional spurs could be effectively eliminated. The ∑Δ modulator also supports high frequency accuracy, large adjustment range and fast channel switching speed.

The multi-order MASH structure ∑Δ modulator has the advantages of good stability and easy implementation, and has been widely used. The higher the order of the MASH structure modulator, the stronger the ability to push the originally evenly distributed quantization noise to the high frequency. In order to ensure that the noise pushed to the high frequency can be effectively filtered by the loop filter, the order number of the MASH structure ∑Δ modulator should not exceed the order number of the loop filter. The Z transformation model for a 2-order MASH structure ∑Δ modulator is shown in Fig. 4.

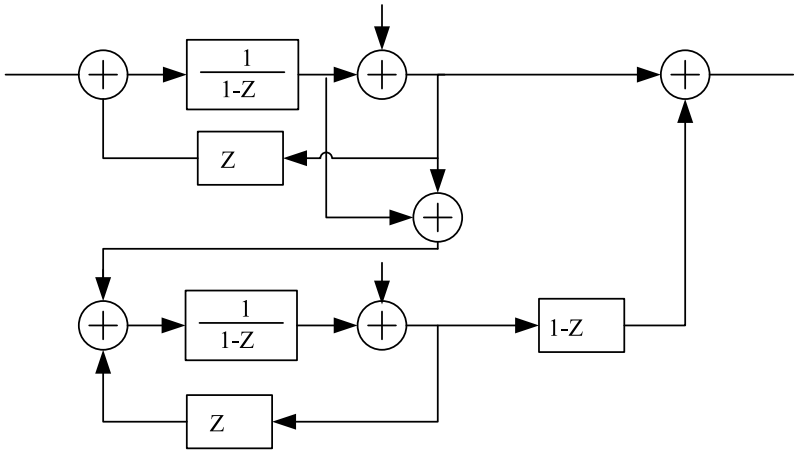

Fig. 4. 2-order MASH structure ∑Δ modulator. *K(Z)* represents input integer, *E1(Z)* and *E2(K)* represents error after 1 bit quantization, *N(Z)* represents output result

3 Results and Discussion

3.1 Phase Noise

In frequency synthesizer design, spurious suppression index is the key to assessing its performance. Because spurious interference directly affects the sensitivity of the receiving system and the overall performance of the system is degraded. The spurious problem in the design of wideband frequency synthesizers will be more prominent. Due to the wide working bandwidth, clutter suppression needs to be considered more in the design. Phase noise is a parameter used to measure the noise performance of an oscillator in frequency synthesizer. Phase noise is equivalent to measuring the spectral purity of an oscillator in the frequency domain. The definition is as shown in equation (5):

$$L(\Delta\omega) = \frac{Pn}{Pc}. \tag{5}$$

In equation (5), *Pc* represents carrier power, *Pn* represents unit bandwidth noise power of carrier offset frequency. The noise linear model of the ∑Δ frequency synthesizer is shown in Fig. 5, and the symbols are shown in Table 1.

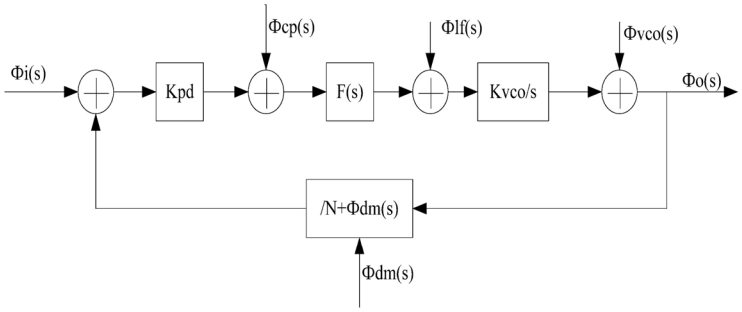

Fig. 5. Schematic diagram of the noise of ∑Δ frequency synthesizer

Table 1. Symbols for the noise of frequency synthesizer

Source noise	Noise from phase detector and charge pump	Voltage noise generated by the loop filter	VCO output noise	∑Δ modulator noise	Overall output noise of the phase-locked loop
Φi(s)	*Φcp(s)*	*Φlf(s)*	*Φvco(s)*	*Φdm(s)*	*Φo(s)*

3.2 Signal Source Noise

The Leeson model is one of the most commonly used models for describing oscillator noise.The model is based on the oscillator test results, and is quite effective for the analysis of the oscillation system. The Leeson model can be expressed by equation (6).

$$S(\Delta f)[dBc/Hz]=10\log[\frac{FkT}{2A}(1+\frac{1}{\Delta f^2}\cdot(\frac{f_0}{2Q})^2)(1+\frac{f_f}{\Delta f})]. \quad (6)$$

In equation (6), f_o represents the carrier frequency, Δf represents the frequency offset, $f_f$represents the flicker noise corner frequency, F represents the oscillator's noise figure, k represents the Boltzmann constant 1.38×10-23J/K, T represents the absolute temperature, and A represents the output power of the oscillation, Q represents the quality factor of the resonant circuit.

According to Fig. 5, each part of the noise will experience different transfer functions, and individually influence the phase-offset phase noise of the PLL output. The transfer function of the signal source noise is shown in equation (7).

$$\frac{\Phi o(s)}{\Phi i(s)}=N\frac{Ho(s)}{1+Ho(s)}. \quad (7)$$

Then the noise contribution of the source noise to the output of the phase-locked loop is as shown in equation (8).

$$S_{i-out}=Si(f)\cdot N^2\cdot\left|\frac{Ho(s)}{1+Ho(s)}\right|^2. \quad (8)$$

The simulation results of the open-loop and closed-loop noise characteristics of a Temperature Compensated Crystal Oscillator (TCXO) signal source are shown in Fig. 6.

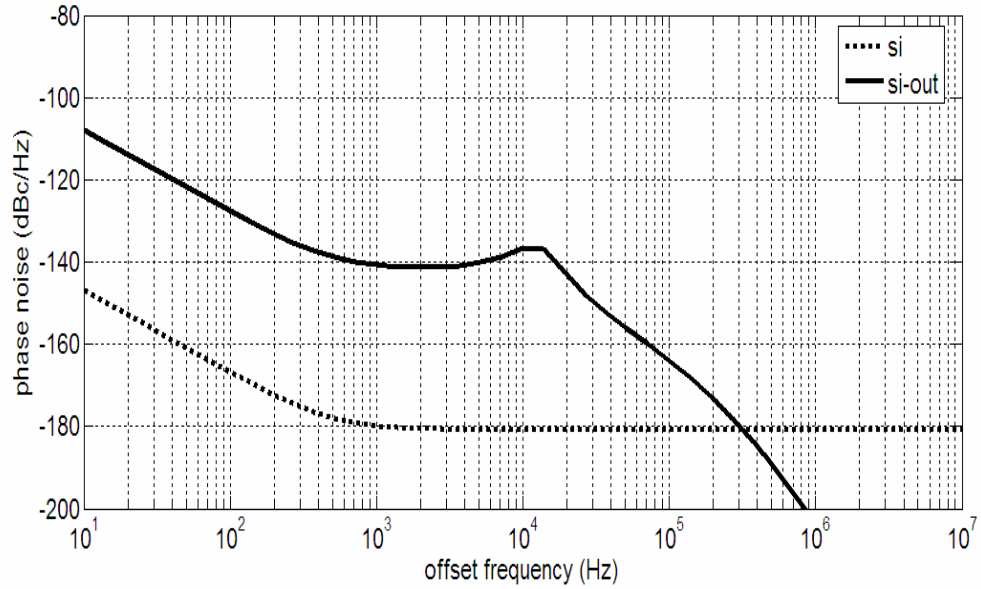

Fig. 6. Open-loop and closed-loop noise of signal source. *Si* represents signal source open-loop noise, and *si-out* represents signal source closed-loop noise

The noise of the reference clock source is generally determined by the noise of the external TCXO oscillator. The noise characteristics are similar to Inductance Capacitor Voltage Controlled Oscillator (LCVCO), but because the Q value of its resonator (about 10000) is much larger than the Q value of the LCVCO resonator, Therefore, its noise performance is much better than that of LCVCO, and its noise floor is generally less than -150dBc/Hz. As can be seen from Fig. 6, the TCXO has a typical low-pass characteristic, and the closed-loop noise is about 20lgN dB higher than the open-loop noise. Therefore, to reduce the noise influence of the signal source, the value of N cannot be too large.

3.3 Loop Filter Noise

The loop filter can be implemented in a passive or active RC network. In a charge-pump type phase-locked loop, in order to reduce the noise caused by the loop filter, it is generally implemented by a passive network. In order to achieve better noise immunity, this design uses a third-order passive filter. According to Fig. 5, the noise transfer function introduced by the loop filter to the PLL output is as shown in equation (9).

$$\frac{\Phi o(s)}{\Phi lf(s)} = \frac{Kvco}{s \cdot (1 + Ho(s))}. \tag{9}$$

The noise contribution of the simulated loop filter to the PLL output is shown in Fig. 6. The total noise power spectrum (*Sall*) curve of the ∑Δ fractional divider is also shown in Fig. 7.

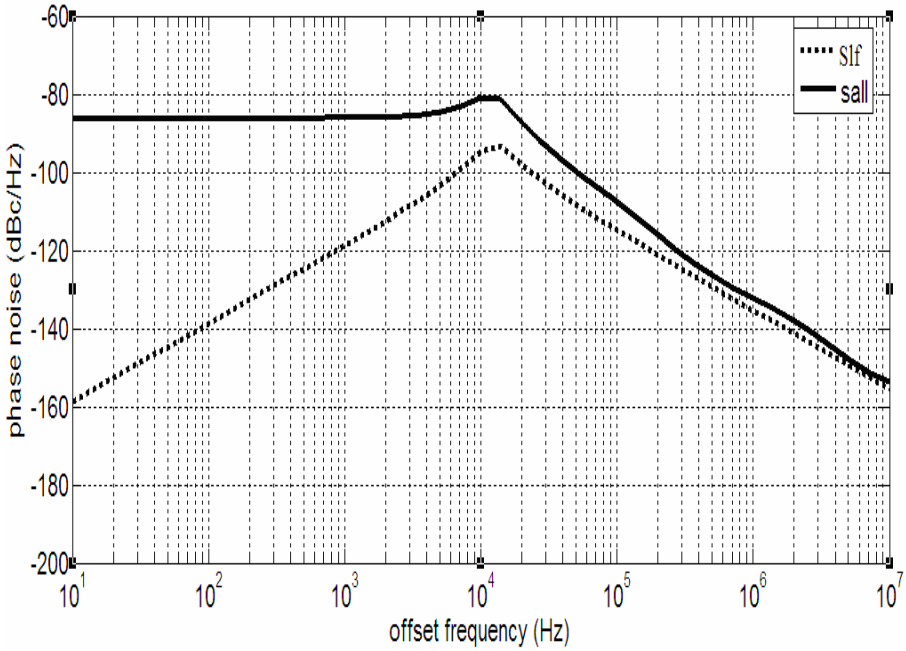

Fig. 7. Noise contribution on PLL output from loop filter. *Slf* represents loop filter noise, *sall* represents PLL all output noise. It can be seen that the loop filter has a significant effect on the PLL noise output in the middle and high frequency bands

3.4 The Noise from Phase Detector and Charge Pump

According to Fig. 5, the noise transfer function of the phase detector and charge pump noise to the PLL output is as shown in equation (10).

$$\frac{\Phi o(s)}{\Phi cp(s)} = \frac{N \cdot Ho(s)}{Kpd \cdot (1 + Ho(s))}. \tag{10}$$

The simulation results of the noise contribution of the phase detector and the charge pump noise to the PLL output are shown in Fig. 8.

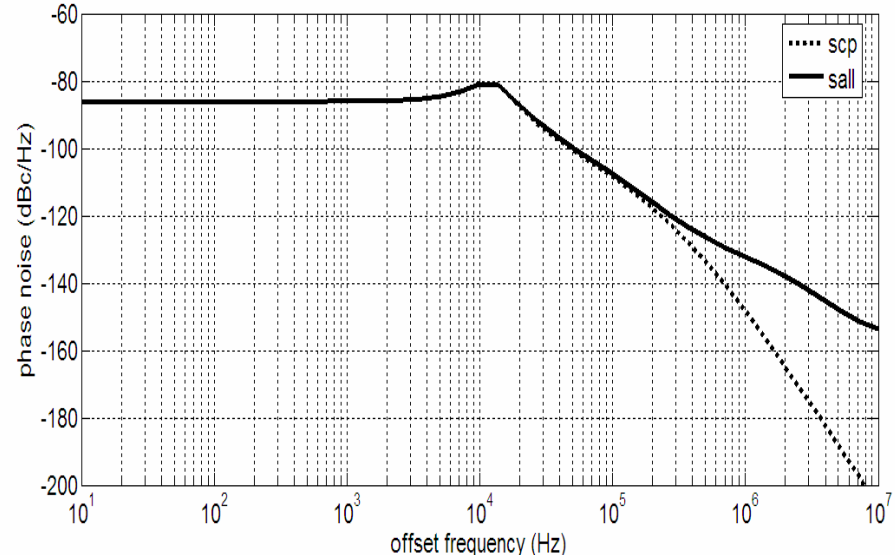

Fig. 8. Noise contribution on PLL output from phase detector and charge pump. *Scp* represents noise from phase detector and charge pump, *sall* represents PLL all output noise. It can be seen that the noises of the phase detector and the charge pump are relatively obvious to the PLL at low frequency, and contribute most of the noise

3.5 VCO Noise

According to Fig. 5, the noise transfer function of the VCO to the PLL output has high-pass characteristics as shown in equation (11).

$$\frac{\Phi o(s)}{\Phi vco(s)} = \frac{1}{(1+Ho(s))}. \tag{11}$$

The noise model of the VCO is basically the same as the reference signal source noise model. However, since the Q value of the LCVCO is smaller, the noise is larger. The simulation results of the noise contribution of LCVCO noise to the PLL output are shown in Fig. 9.

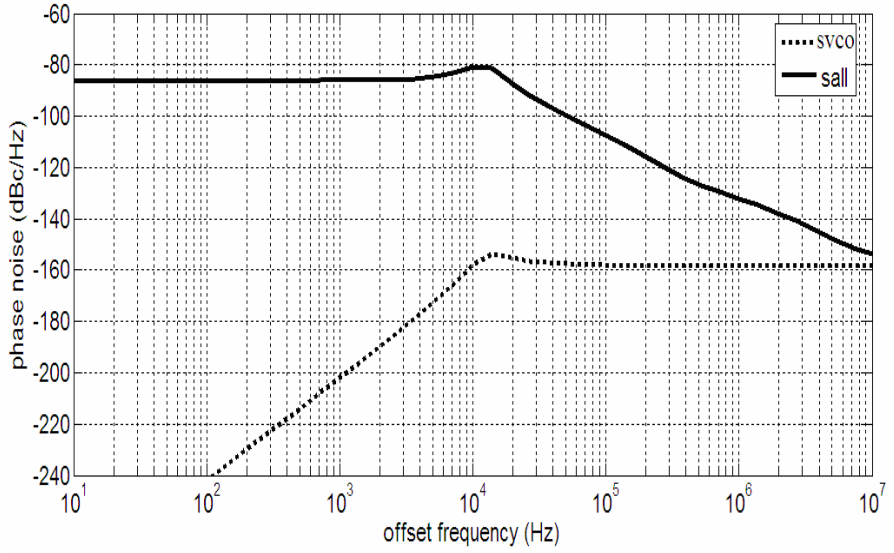

Fig. 9. Noise contribution on PLL output from VCO. *Svco* represents noise from phase detector and charge pump, *sall* represents PLL all output noise. It can be seen that VCO noise is less effective for low-band noise, but has a greater impact on high frequency bands

3.6 ∑Δ Modulator Noise

For the convenience of analysis, the noise transfer function of the ∑Δ modulator also uses the expression of the linear time-invariant system. According to Fig. 5, the noise transfer function of the ∑Δ modulator to the PLL output is as shown in equation (12).

$$\frac{\Phi o(s)}{\Phi dm(s)} = \frac{Ho(s)}{1 + Ho(s)}. \tag{12}$$

The quantization noise of the ∑Δ modulator is amplified by the high-pass shaping of the modulator at a high frequency, and the shape of the output noise spectrum is determined by the noise transfer function of the modulator. In this paper, a 2-order MASH structure ∑Δ modulator is used, and its noise transmission characteristics are shown in equation (13):

$$S_{\Sigma\Delta}(f) = \frac{4\pi^2}{12 f_{ref}} \left|1 - Z^{-1}\right|^2. \tag{13}$$

Then the noise characteristic of the ∑Δ modulator to the phase-locked loop output is as shown in equation (14).

$$S_{dm}(f) = \frac{4\pi^2}{12 f_{ref}} \left|1 - Z^{-1}\right|^2 \left|\frac{Ho(s)}{1 + Ho(s)}\right|^2. \tag{14}$$

The noise contribution of the ∑Δ modulator's quantization noise to the PLL output is shown in Fig. 10.

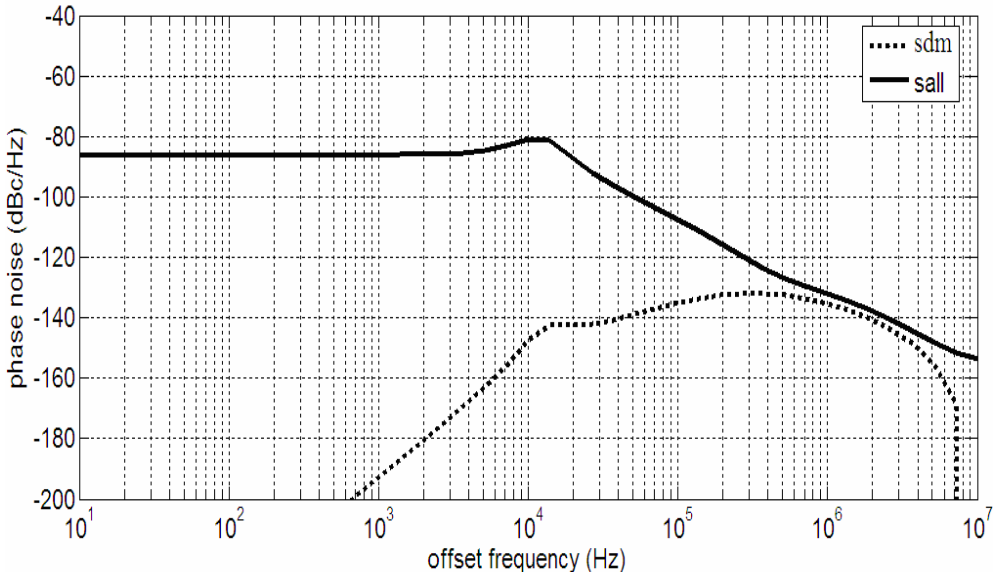

Fig. 10. Noise contribution on PLL output from Quantization noise of ∑Δ frequency synthesizer. *Sdm* represents noise from quantization noise of ∑Δ modulator, *sall* represents PLL all output noise. It can be seen that ∑Δ Modulator noise has a significant effect on the mid-band noise

3.7 Experimental Results for Overall Output Noise

In summary, the phase noise contribution decomposition diagram of each component in the PLL is shown in Fig. 11.

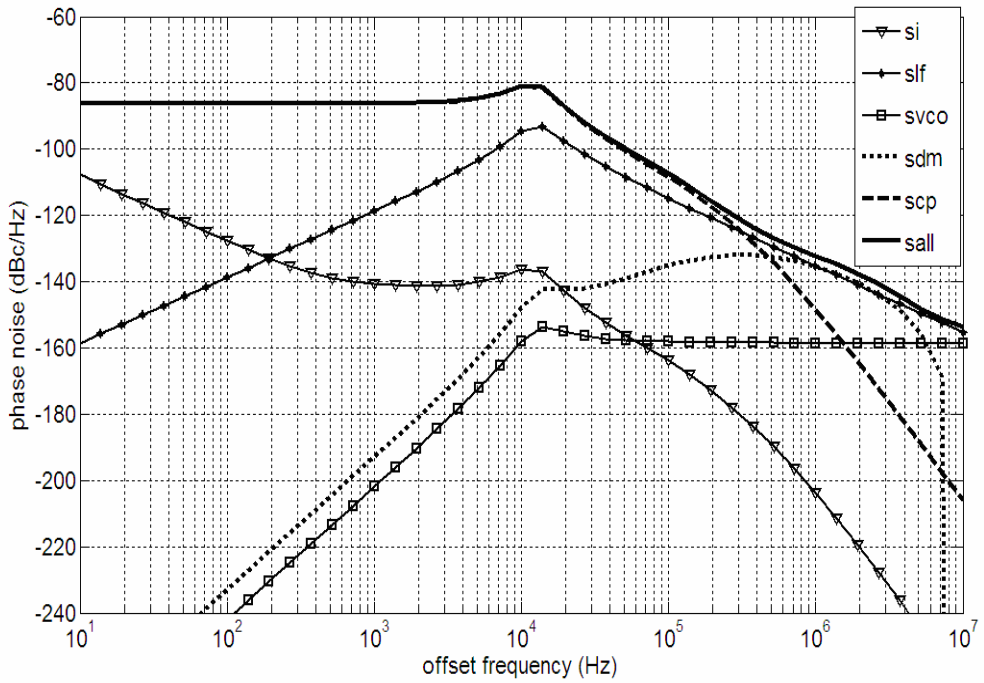

Fig. 11. Phase noise contribution from every component of PLL. *Si* represents signal source open-loop noise, *slf* represents loop filter noise, *scp* represents noise from phase detector and charge pump, *Svco* represents noise from phase detector and charge pump, *Sdm* represents noise from quantization noise of ∑Δ modulator, *sall* represents PLL all output noise

The overall noise curve shows that the noise in the low frequency band is mainly determined by the TCXO, the phase detector and the charge pump, while the high frequency band is basically determined by the VCO, while in the middle frequency band, the noise of the chirp modulation plays a large role.

As can be seen from Fig. 11, the phase noise is -116dBc/Hz at 200 kHz and -132dBc/Hz at 1 MHz. According to the procedure of ETSI EN 302 208-l, the phase noise value require of the frequency synthesizer must be less than -104dBc/Hz@200kHz, -125dBc/Hz@1MHz. So, it can be seen that the design can fully not only meet the above-mentioned RFID requirements for the frequency synthesizer, but also has enough margin space.

4 Conclusions

The low noise frequency synthesizer is the key to the design of RFID readers, and its phase noise performance directly affects the sensitivity and signal to noise ratio of the receiver. The simulation results show that the components of the frequency synthesizer have their own effects on different frequency bands of phase noise. To reduce low frequency noise, the division ratio of the PLL can be reduced. By improving the voltage controlled oscillator and using a higher Q resonant circuit, high frequency noise can be reduced. Reasonable design of the parameters of the loop filter can effectively suppress the noise in the middle and high frequency bands.

Conventional divider quantization noise is evenly distributed throughout the bandwidth. ΔΣ modulation has the characteristics of randomizing the frequency division ratio to push the quantization noise to the high frequency band, which is the noise shaping effect. Moreover, the higher the order value, the stronger the ability of the ΔΣ modulator to shift the noise to the high frequency band. Due to the low-pass characteristics of the loop filter, noise that is transferred to the high frequency band will be filtered out, therefore, fractional spurs could be effectively eliminated. The ∑Δ modulator is used to shape the noise, and the frequency divider quantization noise distribution is changed to reduce the medium-band phase noise.

Acknowledgements

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